S.E. Semester –III

Choice-Based Credit Grading Scheme with Holistic and Multidisciplinary Education (CBCGS-HME 2023)

B.E. (Electronics and Telecommunication Engineering)										**SEM: III**
Course Name: Applied Mathematics III										**Course Code:** BSC-ETC 301
Contact Hours Per Week: 04										**Credits: 04**
Teaching Scheme (Program Specific)					**Examination Scheme (Formative/ Summative)**					
Modes of Teaching / Learning / Weightage					**Modes of Continuous Assessment / Evaluation**					
Hours Per Week					**IA (40)**		**Theory (60)**	**Practical/Oral (25)**	**Term Work (25)**	**Total**
Theory	**Tutorial**	**Practical**	**Contact Hours**	**Credits**	**ISE**	**IE**	**ESE**	**PR**	**TW**	**125**
3	1	-	4	4	20	20	60	-	25	
ISE: In-Semester Examination - Paper Duration – 1 Hours **IE: Innovative Examination** **ESE: End Semester Examination - Paper Duration - 2 Hours** **The weightage of marks for continuous evaluation of Term work/ Report:** Formative (40%), Timely completion of practical (40%) and Attendance/Learning Attitude (20%)										
Prerequisite: Mathematics I, Mathematics II .										

Course Objective:

The course intends to familiarize the prospective engineers with techniques in Laplace Transform Fourier Transform, Z- Transform, Wavelet Transform, Fourier series and Linear algebra (Vector Spaces). It aims to equip the students with standard concepts and tools at an intermediate to advanced level that will serve them well towards tackling more advanced level of mathematics and applications that they would find useful in their disciplines

Course Outcomes: Upon completion of the course students will be able to:

Detailed Syllabus:

Module No.	Topics	Hrs.	Cognitive levels of attainment as per Bloom's Taxonomy
1	**Laplace Transform -I** Laplace transform of standard functions, Properties of Laplace Transform- Linearity, First shifting, change of scale, multiplication by t, division by t, derivative and Integral, Laplace transform of periodic functions, Evaluation of integrals by Laplace transform, Laplace Transform of periodic function, Heaviside function, Dirac delta function.	8	L1, L2, L3
2	**Laplace Transform -II** Finding inverse Laplace transform by First shifting theorem, Partial fractional methods, convolution theorem, inverse Laplace transform by differentiation, solving ordinary differential equations by Laplace Transform method, Solving integral equation and Integral-differential equation.	7	L1, L2, L3
	Fourier Series		

3	Introduction: Orthogonal and Orthonormal set of functions, Introduction of Dirichlet's conditions, Euler's formulae. Fourier Series of Functions: Exponential, trigonometric functions of any period 2L, even and odd functions, half range sine and cosine series. Complex form of Fourier series.	8	L1, L2, L3
4	**Fourier Transform** Fourier integral representation, Fourier Transform and Inverse Fourier transform of constant and exponential function. First shifting, change of scale, multiplication by t, division by t and its application. Relationship between Fourier and Laplace transform.	7	L1, L2, L3
5	**Z –Transform and Wavelet Transform** **Z-**transform: Z-transform of standard functions such as Z (a^n), properties of Z-transform, inverse by Partial fraction method, Wavelet transform, types of wavelets, properties of wavelets.	7	L1, L2, L3
6	**Linear Algebra: Vector Spaces** Vector Space- examples & properties, Subspace, Basis, Dimensions, linear dependence and independence, Linear Transformations (maps), Linear operator, Range and kernel of linear transformation, Matrix of a linear transformation.	8	L1, L2, L3
	Total Hours	**45**	

Online References:

Sr. No.	Website Name	URL	Modules covered
1	http://nptel.ac.in	https://nptel.ac.in/courses/111108066/8	M6
2	www.swayam.gov.in	https://swayam.gov.in/nd1_noc19_ma20/preview	M1, M2, M4
3	www.edx.org	https://www.edx.org/course/differential-equations-fourier-series-and-partial-differential-equations	M3

S.E. Semester –III

Choice-Based Credit Grading Scheme with Holistic and Multidisciplinary Education (CBCGS-HME 2023)

<table>
<tr><td colspan="9">B.E. (Electronics and Telecommunication Engineering)</td><td colspan="3">SEM:
III</td></tr>
<tr><td colspan="9">Course Name: Network and Control Engineering</td><td colspan="3">Course Code: ESC-ETC301</td></tr>
<tr><td colspan="9">Contact Hours Per Week: 05</td><td colspan="3">Credit: 04</td></tr>
<tr><td colspan="5">Teaching Scheme (Program Specific)</td><td colspan="7">Examination scheme</td></tr>
<tr><td colspan="5">Modes of Teaching / Learning / Weightage</td><td colspan="7">Modes of Continuous Assessment / Evaluation</td></tr>
<tr><td colspan="5" rowspan="2">Hours Per Week</td><td colspan="3">Theory (100)</td><td rowspan="2">Practical / Oral / Presentation (25)</td><td rowspan="2">Term Work (25)</td><td rowspan="2">Total</td></tr>
<tr><td colspan="2">IA (40)</td><td>Theory (60)</td></tr>
<tr><td>Theory</td><td>Tutorial</td><td>Practical</td><td>Contact Hours</td><td>Credits</td><td>ISE</td><td>IE</td><td>ESE</td><td>PR/OR</td><td>TW</td><td rowspan="2">150</td></tr>
<tr><td>3</td><td>-</td><td>2</td><td>5</td><td>4</td><td>20</td><td>20</td><td>60</td><td>25</td><td>25</td></tr>
<tr><td colspan="10">ISE: In-Semester Examination- Paper Duration – 1 Hours
IE: Innovative Examinationon
ESE: End Semester Examination-Paper Duration - 2 Hours
The weightage of marks for continuous evaluation of Term work/ Report: Formative (40%), Timely Completion of practical (40%) and Attendance/Learning Attitude (20%)</td></tr>
<tr><td colspan="10">Prerequisite: Basic Electrical Engineering
RBT: Revised Bloom’s Taxonomy</td></tr>
</table>

Course Objective:

The course aims to make the students analyze circuits using KVL and KCL and develop the ability to solve different equations for a given circuit. Student should characterize a given network using different network parameters, learn stability of the network. The course will be useful for students from major streams of engineering to build foundations of time/frequency analysis of systems as well as the feedback control of such systems.

Course Outcomes: Upon completion of the course students will be able to:

Sr. No.	Course Outcomes	Cognitive levels of attainment as per Bloom’s Taxonomy
1	Analyze the basic DC circuits using Mesh and Nodal Analysis and theorems with controlled sources	L1, L2, L3, L4
2	Analyze the transient response using classical methods and Laplace Transform approach for RL, RC, and RLC circuit,	L1, L2, L3
3	Analyze the network in terms of all network parameters and functions	L1, L2, L3, L4
4	Define and compare open loop and closed loop system and Find transfer functions for given system using various methods.	L1, L2, L3
5	Predict stability analysis in time domain using Root locus Analysis	L1, L2, L3, L4
6	Predict stability analysis in frequency domain using various criteria.	L1, L2, L3, L4

Detailed Syllabus:

Module No.	Topics	Hrs.	Cognitive levelsof attainment as
1	**CIRCUIT ANALYSIS AND THEOREMS**	**08**	L1, L2, L3
	Introduction to dependentsources and analyze a Network with Mesh, Super mesh, Node and Super Node analysis (DC analysis only), Circuit Analysis techniques: Superposition, Thevenin's, Norton's, Maximum Power transfer theorems.		
2	**TRANSIENTS IN RC, RL AND RLC CIRCUITS**	**10**	L1, L2, L3, L4
	Network equations using classical method for R-L, R-C circuits andTime Constant, Time domain analysis of R-L-C Circuits: Forced and natural response, effect of damping factor. Solution using second order equation for standard signals, Frequency domain analysis: Frequency- domain representation of R, L, C, applications of Laplace Transform in analyzing electrical circuits		
3	**INTRODUCTION TO NETWORK PARAMETERS AND FUNCTIONS**	**07**	L1, L2, L3, L4
	Two port parameters: Z, Y, H and Transmission parameters, conditions for reciprocity and symmetry (no derivation expected) Network functions for the one port and two port, Driving point function Poles and zeroes of network functions, Time domain behavior asrelated to the Pole-Zero		
4	**INTRODUCTION TO CONTROL SYSTEM ANALYSIS**	**04**	L1, L2, L3, L4
	Definition of system, control, control system, Basic control system components; Feedback principle, Types of control system, Open and closed loop systems, example of control systems. Time response analysis of first and second order control System. Representation of Control System: Signal flow graph, Mason's gain rule.		
5	**STABILITY ANALYSIS IN TIME DOMAIN**	**08**	L1, L2, L3, L4
	Concept of stability: Introduction to stability, Routh and Hurwitz stability criterion. Root locus Analysis: Root locus concept, general rules for constructing root locus, root locus analysis of control system, concept of design of lag and lead compensator.		
6	**STABILITY ANALYSIS IN FREQUENCY DOMAIN**	**08**	L1, L2, L3, L4
	Frequency domain specification, Relationship between time and frequency domain of system, stability margins specification Bode Plot: Magnitude and phase plot, Method of plotting Bode plot, Stability analysis by using Gain and phase margins on the Bode plots. Polar Plot: Concept of Polar plot, Stability from Polar plot		
	Total Hours	**45**	

Books and References:

S.No	Title	Authors	Publisher	Edition	Year
1	Network analysis	Van, Valkenburg	McGraw Hill	9th Edition,	2017
2	Circuits and Network	Sudhakar, A., Shyammohan, S. P	McGraw Hill.	4th Edition	2011
3	Control System Engineering	Nagrath J., and Gopal M	New Age International Publishers	5th Edition	2007
4	Modern Control Engineering	Ogata.K	Prentice Hall of India	5th Edition	2010

Online References:

S. No.	Website Name	URL	Modules Covered
1	Basic Electric Circuits (TheOnline Education-Swayam)	https://swayam.gov.in/nd1_noc19_ee36/preview	M1, M3,
2	NPTEL	https://nptel.ac.in/courses/108105065/21	M2
3.	SWAYAM	https://onlinecourses.nptel.ac.in/noc20_ee90/preview	M4 to M6

List of Tutorial:

Practical Number	Type of Experiment	Practical/ Experiment Topic	Hrs	Cognitive levels of attainment as per Bloom's Taxonomy
1.	Basic Experiments	Verification of Mesh and Nodal Analysis	2	L1, L2, L3, L4
2.		Verification of Thevenin's Theorem	2	L1, L2, L3, L4
3.		Verification of Superposition Theorem	2	L1, L2, L3, L4
4.		Determination of z parameters (dc only) for a network	4	L1, L2, L3
5.		Analyze open loop and closed loop control system using Xcos.	4	L1, L2, L3
6.	Design Experiments	To plot graph for current in RLC circuit for different values of damping factor.	2	L1, L2, L3, L4
7.		Determination of transient response of currentin RL and RC circuit with step voltage input and verify time constant	4	L1, L2, L3,L4
8.		To study frequency response analysis for Various Transfer Function Using Bode Plot	4	L1, L2, L3, L4, L5, L6
9.		To analysis Root Locus for given open loop transfer function	4	L1,L2,L3,L4

10.	**Advanced Experiments**	Analyze second order control System for different types of input signal.	2	L1,L2,L3,L5, L6
		Total Hours	**30**	

S.E. Semester –III

Choice Based Credit Grading Scheme with Holistic and Multidisciplinary Education (CBCGS-HME 2023)

B.E. (Electronics and Telecommunication Engineering)								**SEM:** III		
Course Name: Electronic Device and Circuits								**Course Code: PCC-**ETC 301		
Contact Hours Per Week: 06								**Credits:** 05		
Teaching Scheme (Program Specific)					**Examination Scheme (Formative ve /Summative)**					
Modes of Teaching / Learning / Weightage					**Modes of Continuous Assessment / Evaluation**					
Hours Per Week					**Theory (100)**			**Practical/Oral (25)**	**Term Work (25)**	**Total**
Theory	**Tutorial**	**Practical**	**Contact Hours**	**Credits**	**ISE**	**IE**	**ESE**	**PR**	**TW**	**150**
3	1	2	6	5	20	20	60	25	25	
ISE: In-Semester Examination - Paper Duration – 1 Hours **IE: Innovative Examination on** **ESE: End Semester Examination on - Paper Duration - 2 Hours** **The weightage of marks for continuous evaluation of Term work/ Report:** Formative (40%), Timely completion of practical (40%) and Attendance/Learning Attitude (20%)										
Prerequisite: Intermediate Science level knowledge of Atomic Structure, Physics and BEE **RBT:** Revised Bloom's Taxonomy										

Course Objective:

The course intends to impart fundamental knowledge and application of semiconductor devices like P-N junction, BJT and FET. Students will develop the logical and analytical skills needed to design the amplifier circuits using BJT and FET.

Course Outcomes: Upon completion of the course students will be able to:

SN	Course outcomes	Cognitive levels of attainment as per PI
1	Apply knowledge of science to explain the characteristics of semiconductor devices and its application to solve engineering problems.	L1, L2, L3, L4
2	Apply knowledge of science to explain the characteristics, construction and working of BJT. Identify the best stable circuit for BJT amplifiers.	L1, L2, L3, L4
3	Apply knowledge of science to explain the characteristics, construction and working of FET. Identify the best stable circuit for MOSFET amplifiers.	L1, L2, L3, L4
4	Analysis of BJT amplifiers and MOSFET amplifiers	L1, L2, L3,L4
5	Design BJT and MOSFET amplifiers for any gain and bandwidth.	L1, L2, L3, L4, L5, L6
6	Understand, identify, and differentiate various configurations for specific multistage amplifier.	L1, L2, L3, L4

Detailed Syllabus:

Module No.	Topics	Hrs.	Cognitive levels of attainment as per Bloom's Taxonomy
1	**Diodes and their Applications** PN junction diode and its small signal model, Wave shaping Techniques-Clipper and Clamper, Current and Voltage in an Illuminated Junction, Solar Cells, Photodetectors, Light Emitting Diode: Light Emitting materials, Zener Diode characteristics and applications of Zener diode	7	L1, L2
2	**Bipolar Junction Transistor** Characteristics, construction and working of BJT, DC/AC load line, Q point, Stability, various biasing circuits (Fixed bias and Voltage Divider bias), Emitter bias, Collector to base bias, effect of load and source resistance on CE amplifier.	8	L1, L2, L3, L4
3	**Field Effect Transistors** Characteristics, construction and working of JFET and MOSFET, biasing circuits of MOS. The Depletion-Type MOSFET, Effect of bypass capacitor on MOS Amplifier.	8	L1, L2, L3, L4
4	**Small signal analysis of BJT and MOSFET** **Small signal analysis of BJT -** Small signal model of BJT, BJT as Amplifier, Small signal analysis (Zi, Zo, Av and Ai) of CE amplifier, Effect of bypass capacitor on CE Amplifier **Small signal analysis of MOS -** Small Signal Operation and Models of MOS, MOSFET as an Amplifier and as a Switch Single-Stage MOS Amplifier, Effect of bypass capacitor and effect of load and source resistance on CS Amplifier.	10	L1, L2, L3, L4
5	**Design of Small Signal Amplifiers** Design of single stage BJT and MOS amplifier to obtain desired output voltage and gain.	6	L1, L2, L3, L4, L5, L6
6	**Multistage amplifiers** Apply the knowledge of engineering fundaments to explain Coupling techniques, analyze Cascade amplifiers, Cascode amplifier and Darlington amplifiers	6	L1, L2, L3, L4
	Total Hours	**45**	

Books and References:

SN	Title	Authors	Publisher	Edition	Year
1	Electronic Circuit Analysis and Design	D. A. Neamen	Tata McGraw Hill	2nd Edition	2005
2	Electronic Devices and Circuits	R. S. Dudhe and M.Farhan	Synergy Knowledgeware.	1st Edition	2013
3	Electronic Devices and Circuits Theory	Boylestad and Nashelesky	Pearson Education	11th Edition	2013
4	Integrated Electronics: Analog and Digital Circuits and System	Millman Halkias	McGraw Hill.	2nd Edition	2011
5	Electronic Devices and Circuits; An Introduction	A. Mottershead	Prentice Hall	1st Edition	1973

Online References:

S. No.	Website Name	URL	Modules Covered
1	www.udemy.com	ttps://www.udemy.com/introduction-to-semiconductor-diodes-and-transistors/	M1,M2
2	www.edx.org	https://www.edx.org/course/electronic-materials-and-devices-2	M1-M5
3	www.youtube.com	https://youtu.be/dl66XHbfBcg https://www.youtube.com/watch?v=oMdIzj83qd8 https://youtu.be/c7BbukJpVQE https://youtu.be/aUEwtIgR8ag	M1 M4 M3 M3

Suggested List of Practical/ Experiments:

Practical Number	Type of Experiment	Practical/ Experiment Topic	Hrs.	Cognitive levels of attainment as per Bloom's Taxonomy
1.	Basic Experiments	Study Experiment on testing of cable, Power supply and Function generator / DSO	2	L1, L2
2.		V-I Characteristics of Diode	4	L1, L2, L3, L4
3.		Application of Diode as Clipper circuit	2	L1, L2, L3, L4
4.		Application of diode as Clamper circuit.	4	L1, L2, L3,
5.		Comparison of different Biasing circuit performance for different transistors	2	L4
6.	Design Experiments	Design and verification of single stage BJT amplifier for given gain and bandwidth through simulation.	2	L1, L2, L3, L4, L5, L6
7.		Design and verification of single stage MOS amplifier for given gain and bandwidth through simulation	2	L1, L2, L3, L4, L5, L6
8.	Advanced Experiments	AC parameters of BJT amplifier.	2	L1, L2, L3, L4
9.		AC parameters of Cascode amplifier.	2	L1, L2, L3
10.		AC parameters of MOSFET amplifier.	2	L1, L2, L3, L4
11.		Study Project on electronic devices	4	L1, L2, L3, L4
		Total Hours	**30**	

S.E. Semester-III

Choice Based Credit Grading Scheme with Holistic Multidisciplinary Education (CBCGS-HME 2023)

B.E. (Electronics and Telecommunication Engineering)								**SEM: III**		
Course Name: Digital Logic Design								**Course Code: PCC–ETC 302**		
Contact Hours Per Week: 05								**Credits: 4**		
Teaching Scheme (Program Specific)					**Examination Scheme (Formative / Summative)**					
Modes of Teaching / Learning / Weightage					**Modes of Continuous Assessment / Evaluation**					
Hours Per Week					**Theory (100)**			**Practical Oral (25)**	**Term Work (25)**	**Total**
Theory	**Tutorial**	**Practical**	**Contact Hours**	**Credits**	**ISE**	**IE**	**ESE**	**PR**	**TW**	150
3		2	5	4	20	20	60	25	25	
ISE: In-Semester Examination - Paper Duration — 1 Hours **IE:** Innovative Examination **ESE:** End Semester Examination - Paper Duration - 2 Hours **The weightage of marks for continuous evaluation of Term work/ Report:** Formative (40%), 7imely completion of practical (40%) and Attendance/Learning Attitude (20%)										
Prerequisite: Physics and Applied Mathematics **RBT:** Revised Bloom's Taxonomy										

Course Objective:

The course intends to develop an understanding of number systems and codes and apply the same concepts for inter-conversions. The course also aims to develop an understanding of the analysis of logic processes and implementation of logical operations by applying combinational and sequential logic circuits.

Course Outcomes:

Upon completion of the course students will be able to:

Sr. No.	Course Outcomes	Performance Indicators
1	Apply mathematical techniques and knowledge to solve given problem related to number system and code interconversion and explain various types of codes	PI: 1.1.1 ,1.3.1, 1.4.1 PI: 9.1.2, 9.2.1, 9.2.2 PI: 10.1.1, 10.1.2, 10.2.2, 10.3.1,10.3.2
2	Apply fundamental engineering concepts to simplify Boolean expressions and design using logic gates.	PI: 1.1.1, 1.3.1, 1.4.1 PI: 2.2.4 PI: 9.1.2, 9.2.1, 9.2.2 PI: 10.1.1, 10.1.2, 10.2.2, 10.3.1,10.3.2
3	Analyze and design combinational circuits using electronics engineering concepts, articulate given problem and apply modern engineering tool to implement combinational circuits.	PI: 1.1.1, 1.3.1, 1.4.1 PI: 2.1.1, 2.2.4, 2.4.3 PI: 3.1.5, 3.4.1 PI: 5.1.1, 5.1.2, 5.2.2 PI:9.1.2, 9.2.1, 9.2.2 PI: 10.1, 10.1.2,10.2.2, 10.3.1,10.3.2
4	Compare different logic families and articulate their characteristics.	PI: 1.3.1, 1.4.1 PI: 2.1.1, 2.2.4 PI:9.1.2, 9.2.1, 9.2.2 PI: 10.1, 10.1.2,10.2.2, 10.3.1,10.3.2
5	Analyze and design sequential logic circuits using electronics engineering concepts, articulate given problem and apply engineering concepts to generate diverse set of alternative solutions to state machine design.	PI: 1.1.1, 1.3.1, 1.4.1 PI: 2.1.1, 2.2.4, 2.4.3 PI: 3.1.5, 3.4.1 PI:9.1.2, 9.2.1, 9.2.2 PI: 10.1, 10.1.2,10.2.2, 10.3.1,10.3.2
6	Apply fundamental engineering concepts to design PLDs and compare	PI: 1.2.1, 1.3.1, 1.4.1

	different types of semiconductor memories and articulate their characteristics	PI: 2.1.1, 2.2.1, 2.2.2, 2.2.4 PI:9.1.2, 9.2.1, 9.2.2 PI: 10.1, 10.1.2,10.2.2, 10.3.1,10.3.2

Detailed Syllabus:

Module No	Topics	Hrs.	Cognitive levels of attainment as per Bloom's Taxonomy
1	**Number Systems and Codes** Introduction to number system: Binary, Decimal, Octal arid Hexadecimal, Interconversions, Representation of negative numbers in binary system, Binary Arithmetic. Codes: Weighted & Non-weighted codes, 8-4-2-1 BCD code, Excess -3 code, Gray code, Error detecting and correcting code: Parity code, Hamming code, Alphanumeric codes.	4	L 1, L2, L3
2	**Boolean Algebra and Logic Gates** Boolean identities, Logic Gates and basic logic functions, Inverting and non-inverting buffers, standard forms of logic expressions, simplification of logic expressions using Karnaugh Map (up to 5 variables) and Quine- Me Clues key Methods with Don't Care conditions, Synthesis using AND- OR, NAND, NOR and XOR forms.	6	L 1, L2, L3
3	**Combinational Logic Circuits** Adders, Subtractions, Multiplexers, De-multiplexers, Encoders, Decoders, Code Converters, BCD adder, Magnitude Comparators, Parallel Adder Implementation of Logic expressions using Multiplexers, DE multiplexers, Encoders and Decoders Delay calculation in combinational circuits Case study on VHDL(Implementation of combinational circuits)	10	L 1, L2, L3, L4
4	**Logic families** Brief overview of Transistor as a switch Logic Families — ECL, DTL, RCL, TTL and CMOS Logic gate characteristics — propagation delay, speed, noise margin, fan- out and power dissipation; Standard TTL and CMOS logic gates.	4	L 1, L2
5	**Sequential logic circuits** Latches and Flip Flops (SR, D, JK, 7) with characteristic equations, Master - Slave and Edge triggered Flip-Flops; Direct Preset and Clear Inputs. Shift register - PlPO, SIPO, PISO, SISO, Bi-Directional Shift Registers; Universal Shift register, Applications of shift registers as Ring Counter and Johnson Counter Counters — synchronous, asynchronous, up, down, up/down. Finite State Machines — Analysis and design of Mealy and Moore Machines, State minimization/reduction techniques, State Assignment; Design of Sequence Generators and Sequence Detectors. Propagation delay, setup and hold time, critical path delay.	5	L 1, L2, L3, L4
6	**Semiconductor Memories and Programmable Logic Devices** Semiconductor memories: ROM, SRAM, DRAM. PLDS: Combinational circuits using ROM, PLA and PAL	6	L 1, L2, L3
	Total Hours	**45**	

Books and References:

Sr. No.	Title	Authors	Publisher	Edition	Year
1	An Engineering Approach to Digital Design	W. Fletcher	PHI	Reprint of 1" Edition	2021
2	Digital Logic and Computer Design	Morris Mario	Pearson	Reprint of 1“ Edition	2022
3	Digital Design Principles and Practices	Wakerly J.F.	Pearson India	5th Edition	2018
4	Digital System Design using VHDL	C.H. Roth	Thompson Publications	3rd Edition	2018
5	Modern Digital Electronics	R.P. Jain	McGraw Hill	5th Edition	2022

Online References:

S.No.	Website Name	URL	Modules Covered
1	Tutorials point	https://www.tutorialspoint.com/digital circuits/	Ml, M2, M3, M5
2	Swayam	https://swayam.Nov.in/nd1_noc19_ee51	MI-M5
3	Swayam	https://swayam.Nov.iWnd l_noc l9_cs74/	M 1-M6

Suggested List of Practical/ Experiments:

Practical Number	Type of Experiment	Practical/ Experiment Topic	Hrs.	Cognitive levels of attainment as per Bloom's Taxonomy
1	Basic Experiments	To Verify that NAND & NOR are Universal Gate	2	L 1, L2, L3
2		To Study Conversion of Flip flop (a) JK to T (b) JK to D	2	L1, L2, L3
3	Design Experiments	Design Half Adder & Full Adder using Logic Gates	2	L 1, L2, L3
4		To Implement Logic Expression Using Decoder IC 74138	2	L 1, L2, L3
5		Design & Implement 4-bit synchronous counter using IC 74169	4	L 1, L2, L3
6		Design & Implement of 4-bit shift register (shift right) using IC 7495	2	L 1, L2, L3
7		To design a sequence Generator to Generate the sequence 2,3,1,0	4	L 1, L2, L3
8	Advanced Experiments	To study and Implement Full adder using VHDL	4	L 1, L2, L3, L4
9		To study and Implement Multiplexer using VHDL	4	LI, L2, L3, L4
10		Mini Project	4	LI, L2, L3, L4
		Total Hours	**30**	

S.E. Semester-III

Choice Based Credit Grading Scheme with Holistic Multidisciplinary Education (CBCGS-HME 2023)

B.E. (Electronics and Telecommunication Engineering)								**SEM: III**		
Course Name: Digital Logic Design								**Course Code: PCC –ETC 302**		
Contact Hours Per Week: 05								**Credits: 4**		
Teaching Scheme (Program Specific)					**Examination Scheme (Formative / Summative)**					
Modes of Teaching / Learning / Weightage					**Modes of Continuous Assessment / Evaluation**					
Hours Per Week					**Theory (100)**			**Practical Oral (25)**	**Term Work (25)**	**Total**
Theory	**Tutorial**	**Practical**	**Contact Hours**	**Credits**	**ISE**	**IE**	**ESE**	**PR**	**TW**	150
		2	5	4	20	20	60	25	25	
ISE: In-Semester Examination - Paper Duration — 1 Hours **IE:** Innovative Examination **ESE:** End Semester Examination - Paper Duration - 2 Hours **The weightage of marks for continuous evaluation of Term work/ Report:** Formative (40%), 7imely completion of practical (40%) and Attendance/Learning Attitude (20%)										
Prerequisite: Physics and Applied Mathematics **RBT:** Revised Bloom's Taxonomy										

Course Objective:

The course intends to develop an understanding of number systems and codes and apply the same concepts for inter-conversions. The course also aims to develop an understanding of the analysis of logic processes and implementation of logical operations by applying combinational and sequential logic circuits.

Course Outcomes:

Upon completion of the course students will be able to:

Sr. No.	Course Outcomes	Performance Indicators
1	Apply mathematical techniques and knowledge to solve given problem related to number system and code interconversion and explain various types of codes	L1, L2, L3
2	Apply fundamental engineering concepts to simplify Boolean expressions and design using logic gates.	L1, L2, L3
3	Analyze and design combinational circuits using electronics engineering concepts, articulate given problem and apply modern engineering tool to implement combinational circuits.	L1, L2, L3, L4
4	Compare different logic families and articulate their characteristics.	L1, L2
5	Analyze and design sequential logic circuits using electronics engineering concepts, articulate given problem and apply engineering concepts to generate diverse set of alternative solutions to state machine design.	L1, L2, L3, L4
6	Apply fundamental engineering concepts to design PLDs and compare different types of semiconductor memories and articulate their characteristics	L1, L2, L3

Detailed Syllabus:

Module No	Topics	Hrs.	Cognitive levels of attainment as per Bloom's Taxonomy
1	**Number Systems and Codes** Introduction to number system: Binary, Decimal, Octal arid Hexadecimal, Interconversions, Representation of negative numbers in binary system, Binary Arithmetic. Codes: Weighted & Non-weighted codes, 8-4-2-1 BCD code, Excess -3 code,	4	L1, L2, L3

	Gray code, Error detecting and correcting code: Parity code, Hamming code, Alphanumeric codes.		
2	**Boolean Algebra and Logic Gates** Boolean identities, Logic Gates and basic logic functions, Inverting and non-inverting buffers, standard forms of logic expressions, simplification of logic expressions using Karnaugh Map (up to 5 variables) and Quine- Me Clues key Methods with Don't Care conditions, Synthesis using AND- OR, NAND, NOR and XOR forms.	6	L 1, L2, L3
3	**Combinational Logic Circuits** Adders, Subtractions, Multiplexers, De-multiplexers, Encoders, Decoders, Code Converters, BCD adder, Magnitude Comparators, Parallel Adder Implementation of Logic expressions using Multiplexers, DE multiplexers, Encoders and Decoders Delay calculation in combinational circuits Case study on VHDL (Implementation of combinational circuits)	10	L1, L2, L3, L4
4	**Logic families** Brief overview of Transistor as a switch Logic Families — ECL, DTL, RCL, TTL and CMOS Logic gate characteristics — propagation delay, speed, noise margin, fan- out and power dissipation; Standard TTL and CMOS logic gates.	4	L 1, L2
5	**Sequential logic circuits** Latches and Flip Flops (SR, D, JK, 7) with characteristic equations, Master - Slave and Edge triggered Flip-Flops; Direct Preset and Clear Inputs. Shift register - PlPO, SIPO, PISO, SISO, Bi-Directional Shift Registers; Universal Shift register, Applications of shift registers as Ring Counter and Johnson Counter Counters — synchronous, asynchronous, up, down, up/down. Finite State Machines — Analysis and design of Mealy and Moore Machines, State minimization/reduction techniques, State Assignment; Design of Sequence Generators and Sequence Detectors. Propagation delay, setup and hold time, critical path delay.	5	L 1, L2, L3, L4
6	**Semiconductor Memories and Programmable Logic Devices** Semiconductor memories: ROM, SRAM, DRAM. PLDS: Combinational circuits using ROM, PLA and PAL	6	L 1, L2, L3
	Total Hours	**45**	

Books and References:

Sr. No.	Title	Authors	Publisher	Edition	Year
1	An Engineering Approach to Digital Design	W. Fletcher	PHI	Reprint of 1" Edition	2021
2	Digital Logic and Computer Design	Morris Mario	Pearson	Reprint of 1“ Edition	2022
3	Digital Design Principles and Practices	Wakerly J.F.	Pearson India	5th Edition	2018
4	Digital System Design using VHDL	C.H. Roth	Thompson Publications	3rd Edition	2018
5	Modern Digital Electronics	R.P. Jain	McGraw Hill	5th Edition	2022

Online References:

S.No.	Website Name	URL	Modules Covered
1	Tutorials point	https://www.tutorialspoint.com/digital circuits/	Ml, M2, M3, M5
2	Swayam	https://swayam.Nov.in/nd1_noc19_ee51	MI-M5
3	Swayam	https://swayam.Nov.iWnd l_noc l9_cs74/	M 1-M6

List of Practicals/Experiments:

Practical Number	Type of Experiment	Practical/ Experiment Topic	Hrs.	Cognitive levels of attainment as per Bloom's Taxonomy
1	Basic Experiments	To Verify that NAND & NOR are Universal Gate	2	L 1, L2, L3
2		To Study Conversion of Flip flop (a) JK to T (b) JK to D	2	L1, L2, L3
3	Design Experiments	Design Half Adder & Full Adder using Logic Gates	2	L 1, L2, L3
4		To Implement Logic Expression Using Decoder IC 74138	2	L 1, L2, L3
5		Design & Implement 4-bit synchronous counter using IC 74169	4	L 1, L2, L3
6		Design & Implement of 4-bit shift register (shift right) using IC 7495	2	L 1, L2, L3
7		To design a sequence Generator to Generate the sequence 2,3,1,0	4	L 1, L2, L3
8	Advanced Experiments	To study and Implement Full adder using VHDL	4	L 1, L2, L3, L4
9		To study and Implement Multiplexer using VHDL	4	LI, L2, L3, L4
10		Mini Project	4	LI, L2, L3, L4
		Total Hours	30	